said predetermined value outputted from said multiplier constructing said compensating means is subtracted from an output of said multiplier constructing said phase difference detector and said subordinate filter is controlled by an output of said subtraction, thereby compensating a variation of characteristics of said phase difference detector constructed by said multiplier.--

REMARKS

This Amendment is responsive to the Office Action dated August 14, 2002. Claims 1-7 were pending in the application. In the Office Action claims 1-7 were rejected, and claims 1 and 7 were objected to. In this Amendment, claims 1 and 7 have been amended. Claims 1-7 thus remain for consideration.

Applicant submits that claims 1-7 are in condition for allowance and requests reconsideration and withdrawal of the rejections in light of the following remarks.

Drawings

The drawing objection is noted and is corrected in accordance with the Request for Approval of Drawing Change submitted herewith.

Specification

Applicant has made amendments to the specification and submits that the specification now meets all formality requirements.

Claim Objections

Claims 1 and 7 were objected to on account of informalities.

Applicant has amended claims 1 and 7 as suggested by the Examiner and submits that claims 1 and 7 as amended are in compliance with all formality requirements.

§102 and §103 Rejections

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by Sato (U.S. Patent No. 5,239,367).

Claims 2-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sato.

Applicant submits that claim 1 as amended is patentable over Sato.

Applicant's invention as recited in claim 1 is directed toward a filter apparatus that includes a main filter and a subordinate filter. The claim recites that "a cut off frequency of at least one of said main filter and said subordinate filter is controlled through the value of at least one resistor in said filter and the value of said resistor is set according to an external voltage."

Sato does not disclose controlling the cut off frequency of a filter by setting the value of at least one resistor in the filter according to an external voltage. Accordingly, Applicant believes claim 1 is patentable over Sato on at least this basis.

Claims 2-7 depend on claim 1. Since claim 11 is believed to be patentable over Sato, claims 2-7 are believed to be patentable over Sato on the basis of their dependency on claim 1.

Applicant respectfully submits that all of the claims now pending in the application are in condition for allowance, which action is earnestly solicited.

It is submitted that these claims, as originally presented, are patentably distinct over the prior art cited by the Examiner, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes to these claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes are made simply for clarification and to round out the scope of protection to which Applicant is entitled.

Statements appearing above with respect to the disclosures in the cited references represent the present opinions of the Applicant's undersigned attorney and, in the event that the Examiner disagrees with any such opinions, it is respectfully requested that the Examiner specifically indicate those portions of the respective reference providing the basis for a contrary view.

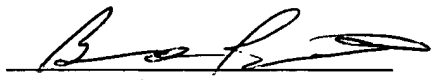
If any issues remain, or if the Examiner has any further suggestions, he/she is invited to call the undersigned at the telephone number provided below.

The Examiner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account No. 50-0320.

The Examiner's consideration of this matter is gratefully acknowledged.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph appearing at page 2, lines 19-25, has been amended as follows:

--According to the super heterodyne system, however, since an image frequency is generated when the RF signal is down-converted into the IF signal, it is necessary to provide [the] a band pass filter for an IF circuit. A [The] SAW filter is used as such a band pass filter. It is, therefore, difficult to form an integrated circuit and it becomes an obstacle to miniaturization.--

The paragraph appearing at page 3, lines 5-10, has been amended as follows:

--In the case of using the direct conversion system, a low pass filter is inserted after the I signal and Q signal are orthogonally demodulated by the multiplier. As such a low pass filter, since the base band signal is directly demodulated, a frequency which is handled is low and it is difficult to use the SAW filter.--

The paragraph appearing at page 11, lines 1-14, has been amended as follows:

--Since the subordinate LPF 21 has the phase characteristics[,] when the signal passes through the subordinate LPF 21, a phase difference according to the phase characteristics is caused between the input signal and the output signal. The signal from the signal generating circuit 22 and the signal from the signal generating circuit 22 in which the phase has been shifted by the passage through the subordinate LPF 21 are supplied to the phase difference detecting

circuit 23. Therefore, the detection value corresponding to the phase shift amount at the time when the signal of the frequency corresponding to the cut-off frequency is supplied to the subordinate LPF 21 is detected by the phase difference detecting circuit 23.--

The paragraph appearing at page 20, line 27 – page 21, line 9 has been amended as follows:

--In the multiplier 25A used as a reference value generating circuit 25, [it is constructed lest the] output is [caused] from the output terminals OUT11 and OUT12 in Fig. 9. For example, no signal is inputted to the input terminals IN11 and IN12 and no signal is inputted to the input terminals IN13 and IN14. The multiplier 23A used as a phase difference detecting circuit 23 and the multiplier 25A used as a reference value generating circuit 25 are arranged at the positions where they are matched on the layout and on the temperature change and processes.--

IN THE CLAIMS

Claims 1 and 7 have been amended as follows:

--1(amended). A filter apparatus comprising:

a main filter which has an input terminal and an output terminal and whose characteristics [can be] <u>is</u> set by an external control signal;

a subordinate filter having substantially the same construction as that of said main filter;

a signal generator for generating a signal of a frequency equal to a cut-off frequency of each of said main filter and said subordinate filter and supplying it to said subordinate filter;

a phase difference detector for detecting a phase difference between the signal generated from said signal generator and an output signal of said subordinate filter and outputting a phase difference signal;

a reference signal generator for generating a reference signal corresponding to an ideal value of the phase difference detected by said phase difference detector; and

an error detector for detecting an error between said phase difference signal and said reference signal and supplying an error signal as said external control signal to said main filter and said subordinate filter;

whereby a cut off frequency of at least one of said main filter and said subordinate filter is controlled through the value of at least one resistor in said filter and the value of said resistor is set according to an external voltage.

7(amended). An apparatus according to claim 6, wherein

said compensating means is a multiplier [similar] substantially similar to the multiplier constructing said phase difference detector,

a predetermined value is generated by said multiplier constructing said compensating means, and

[and] said predetermined value outputted from said multiplier constructing said compensating means is subtracted from an output of said multiplier[s] constructing said phase difference detector and said subordinate filter is controlled by an output of said subtraction, thereby compensating a variation of characteristics of said phase difference detector constructed by said multiplier.--

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Fig. 1
(Prior Art)